Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte ANDRE' SEZNEC

Appeal No. 1998-1506
Application No. 08/302,695

HEARD: November 14, 2000

Before RUGGIERO, DIXON, and GROSS, Administrative Patent Judges.

GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 through 5, which are all of the claims pending in this application.

Appellant's invention relates to a cache memory device. Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. An improved cache memory device for use in a data processing system which includes an addressable main memory (MP); at least one request input/output (ESRQ) for receiving a request (REQ) for access to a data item stored in the

addressable main memory (MP) or in the cache memory device, the request (RQ) including a main address (AP) of the desired data item; at least one main memory input/output (ESMP) connected to the main addressable memory (MP) for accessing the desired data item of the main memory; a plurality of X memory banks (BCi) with i being less than or equal to X and greater than 0, each having a number Li of lines capable of containing data, these lines being capable of being individually designated by a local address (ALi) in each bank (BCi); computing means (CAL) connected to the request input/output (ESRQ) and capable of answering the request (REQ) by transforming the main address (AP) contained in this request to a local address (AL) inside each of the banks (BCi), the line thus designated in the bank (BCi) being the only line of the said bank that is capable of containing the data labelled by the main address; and loading means (CHA) connected to the main memory input/output (ESMP) for loading the data line of the main memory containing the desired data item into the cache memory device if it is not present in the cache memory device, wherein the improvement comprises:

the computing means (CAL) comprises means for transforming the main address (AP) into a first local address in a first one of the memory banks in accordance with a first predetermined law associated with the first one of the memory banks, and for transforming the main address (AP) into a second local address in a second one of the memory banks in accordance with a second predetermined law which is associated with the second one of the memory banks,

the first and second predetermined laws are distinct, and

the first and second memory banks are addressed separately, according to their respective law.

The prior art reference of record relied upon by the examiner in rejecting the appealed claims is:

Melton et al. (Melton) 5,133,061 Jul. 21, 1992

Claims 1 through 5 stand rejected under 35 U.S.C. § 103 as being unpatentable over Melton.

Reference is made to the Examiner's Answer (Paper No. 15, mailed August 8, 1997) for the examiner's complete reasoning in support of the rejection, and to appellant's Brief (Paper No. 14, filed April 14, 1997) and Reply Brief (Paper No. 16, filed October 8, 1997) for appellant's arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art reference, and the respective positions articulated by appellant and the examiner. As a consequence of our review, we will reverse the obviousness rejection of claims 1 through 5.

Claim 1 requires, in pertinent part, a plurality of memory banks and a "means for transforming the main address (AP) into a first local address in a first one of the memory banks in accordance with a first predetermined law ... and ... into a second local address in a second one of the memory banks in accordance with a second predetermined law." Appellant contends (Brief, page 8) that "Melton uses a single law to transform a main address into a single local address

for a plurality of columns in his cache." Further, appellant adds (Brief, page 9) that in Melton's system, one mapping law is used for all of the columns (or banks), and "a particular main memory address is transformed into the same local address in each of Melton's columns." We agree. Melton uses a single mapping matrix as exemplified in Figure 6 regardless of the column or bank. Therefore, a single mapping function is used for all cache memory banks.

The examiner seems to admit that Melton fails to disclose a different mapping law for each bank by stating (Answer, pages 6-7) that "it would have been obvious ... to improve CPU utilization ... by maximizing the useful data or instructions that remain in the cache by reducing thrashing by creating [sic, or] using different mapping algorithms." Yet, the examiner provides no support for a conclusion that plural mapping laws would have been obvious. Further, the examiner asserts (Answer, page 8) that Melton's mapping function is different because "the matrix multiply is performed on different bits of the address." In other words, the examiner apparently believes that if each bit is multiplied by a different number, then there are plural mapping functions.

However, the examiner's focus on individual bits within an address is misplaced, as the claim requires a different mapping function for each memory bank. As explained above, each column, or memory bank, of Melton uses the same matrix, and thus the same mapping function. Accordingly, we cannot sustain the rejection of claim 1 or its dependents, claims 2 through 5.

CONCLUSION

The decision of the examiner rejecting claims 1 through 5 under 35 U.S.C. § 103 is reversed.

REVERSED

JOSEPH F. RUGGIERO Administrative Patent Judge	)
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ANITA PELLMAN GROSS Administrative Patent Judge	)

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